WEST

| Help | Logout | Interrupt |

| Main Menu | Search Form | Posting Counts | Show S Numbers | Edit S Numbers | Preferences | Cases |

Search Results -

Term	Documents
DISTANCE.USPT.	859783
DISTANCES.USPT.	150325
RELATION$6	0
RELATION.USPT.	549175
RELATIONAHIP.USPT.	42
RELATIONAL.USPT.	7164
RELATIONALAS.USPT.	2
RELATIONALIZE.USPT.	1
RELATIONALLY.USPT.	184
RELATIONALS.USPT.	2
RELATIONALY.USPT.	1
((DISTANCE OR RELATION$6) NEAR8 EFFECTIVE NEAR1 ADDRESS$3).USPT.	22

There are more results than shown above. Click here to view the entire set.

Database:

```
US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins
```

Search: L13

| Refine Search |

| Recall Text ⬍ | Clear |

Search History

DATE: Thursday, May 30, 2002   Printable Copy   Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L13	(distance or relation$6) near8 effective near1 address$3	22	L13
L12	compar$6 near8 effective near1 address$3	228	L12
L11	hash near8 effective near1 address$3	5	L11
L10	relative near4 (address or distance) near9 effective near1 address$3	54	L10
L9	(comput$3 or calculat$3) near4 effective near3 address$3 near8 instruction$ near5 (first or second)	43	L9
L8	(comput$3 or calculat$3) near4 effective near3 address$3 near8 instruction$	315	L8
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L7	effective near3 address$3 near8 (first or second) near7 (relative or relation$ or relationship)	13	L7
L6	effective near3 address$3 near8 (first or second)	577	L6
L5	effective near3 address$3 near8 location$ near15 (relative or relationship$) near5 address$3	10	L5
L4	effective near3 address$3 location$ near15 (relative or relationship$) near5 address$3	6377	L4
L3	effective near3 address$3 near5 instruction$ near8 (relative or relationship$) near5 address$3	12	L3
L2	effective near3 address$3 near8 (relative or relationship$) near5 address$3	93	L2
L1	effective near3 address$3 and (relative or relationship$) near5 address$3	722	L1

END OF SEARCH HISTORY

WEST

Freeform Search

Database:

```
US Patents Full-Text Database
US Pre-Grant Publication Full-Text Database
JPO Abstracts Database
EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins
```

Term:

Display: `20` Documents in <u>Display Format</u>: `TI` Starting with Number `1`

Generate: ○ Hit List ● Hit Count ○ Side by Side ○ Image

| Search | Clear | Help | Logout | Interrupt |

| Main Menu | Show S Numbers | Edit S Numbers | Preferences | Cases |

Search History

DATE: **Thursday, May 30, 2002**   <u>Printable Copy</u>   <u>Create Case</u>

<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L7</u>	effective near3 address$3 near8 (first or second) near7 (relative or relation$ or relationship)	13	<u>L7</u>
<u>L6</u>	effective near3 address$3 near8 (first or second)	577	<u>L6</u>
<u>L5</u>	effective near3 address$3 near8 location$ near15 (relative or relationship$) near5 address$3	10	<u>L5</u>
<u>L4</u>	effective near3 address$3 location$ near15 (relative or relationship$) near5 address$3	6377	<u>L4</u>
<u>L3</u>	effective near3 address$3 near5 instruction$ near8 (relative or relationship$) near5 address$3	12	<u>L3</u>
<u>L2</u>	effective near3 address$3 near8 (relative or relationship$) near5 address$3	93	<u>L2</u>
<u>L1</u>	effective near3 address$3 and (relative or relationship$) near5 address$3	722	<u>L1</u>

END OF SEARCH HISTORY

WEST

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Search Results - Record(s) 1 through 20 of 43 returned.

☐ 1. Document ID: US 6334176 B1

L9: Entry 1 of 43   File: USPT   Dec 25, 2001

US-PAT-NO: 6334176
DOCUMENT-IDENTIFIER: US 6334176 B1

TITLE: Method and apparatus for generating an alignment control vector

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 2. Document ID: US 6163836 A

L9: Entry 2 of 43   File: USPT   Dec 19, 2000

US-PAT-NO: 6163836
DOCUMENT-IDENTIFIER: US 6163836 A

TITLE: Processor with programmable addressing modes

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 3. Document ID: US 6151673 A

L9: Entry 3 of 43   File: USPT   Nov 21, 2000

US-PAT-NO: 6151673
DOCUMENT-IDENTIFIER: US 6151673 A

TITLE: Data processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 4. Document ID: US 6128703 A

L9: Entry 4 of 43   File: USPT   Oct 3, 2000

US-PAT-NO: 6128703
DOCUMENT-IDENTIFIER: US 6128703 A

TITLE: Method and apparatus for memory prefetch operation of volatile non-coherent

data

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |

Draw Desc | Image

☐ 5. Document ID: US 5996057 A

L9: Entry 5 of 43   File: USPT   Nov 30, 1999

US-PAT-NO: 5996057
DOCUMENT-IDENTIFIER: US 5996057 A

TITLE: Data processing system and method of permutation with replication within a
vector register file

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |

Draw Desc | Image

☐ 6. Document ID: US 5978904 A

L9: Entry 6 of 43   File: USPT   Nov 2, 1999

US-PAT-NO: 5978904
DOCUMENT-IDENTIFIER: US 5978904 A

TITLE: Data processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |

Draw Desc | Image

☐ 7. Document ID: US 5930509 A

L9: Entry 7 of 43   File: USPT   Jul 27, 1999

US-PAT-NO: 5930509
DOCUMENT-IDENTIFIER: US 5930509 A

TITLE: Method and apparatus for performing binary translation

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |

Draw Desc | Image

☐ 8. Document ID: US 5913054 A

L9: Entry 8 of 43   File: USPT   Jun 15, 1999

US-PAT-NO: 5913054
DOCUMENT-IDENTIFIER: US 5913054 A

TITLE: Method and system for processing a multiple-register instruction that permit
multiple data words to be written in a single processor cycle

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 9.   Document ID: US 5884060 A

L9: Entry 9 of 43   File: USPT   Mar 16, 1999

US-PAT-NO: 5884060
DOCUMENT-IDENTIFIER: US 5884060 A

TITLE: Processor which performs dynamic instruction scheduling at time of execution
within a single clock cycle

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☑ 10.   Document ID: US 5881307 A

L9: Entry 10 of 43   File: USPT   Mar 9, 1999

US-PAT-NO: 5881307
DOCUMENT-IDENTIFIER: US 5881307 A

TITLE: Deferred store data read with simple anti-dependency pipeline inter-lock
control in superscalar processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 11.   Document ID: US 5860154 A

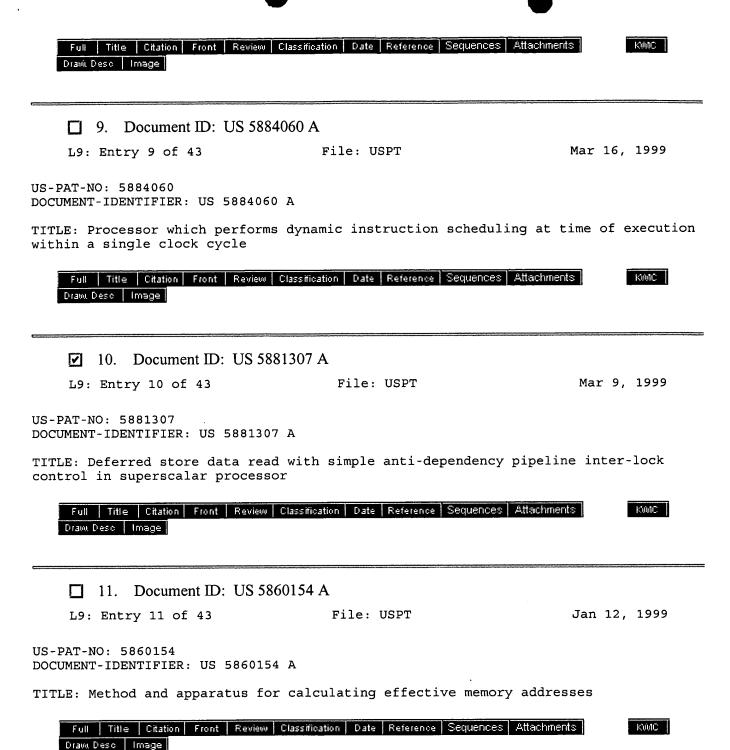L9: Entry 11 of 43   File: USPT   Jan 12, 1999

US-PAT-NO: 5860154
DOCUMENT-IDENTIFIER: US 5860154 A

TITLE: Method and apparatus for calculating effective memory addresses

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC |
| Draw Desc | Image |

☐ 12.   Document ID: US 5854913 A

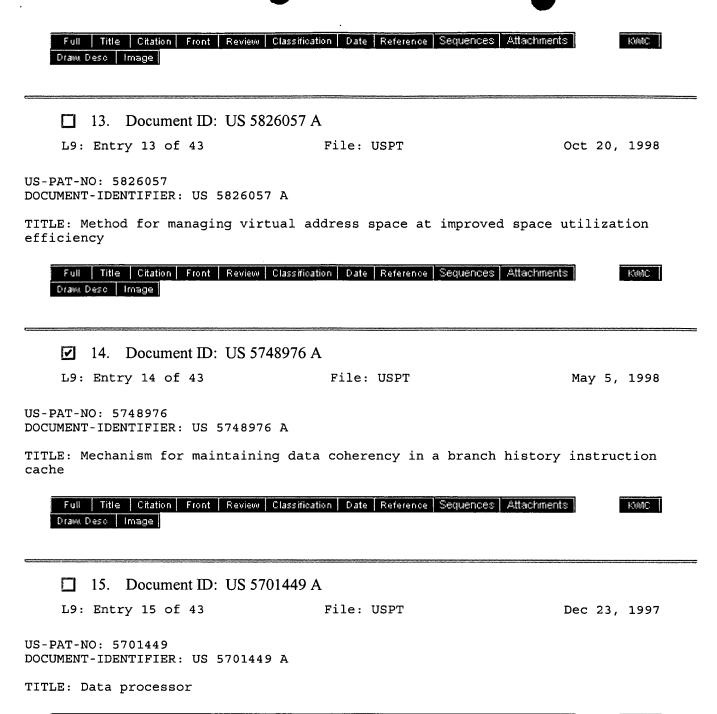L9: Entry 12 of 43   File: USPT   Dec 29, 1998

US-PAT-NO: 5854913
DOCUMENT-IDENTIFIER: US 5854913 A

TITLE: Microprocessor with an architecture mode control capable of supporting
extensions of two distinct instruction-set architectures

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |
| Draw Desc | Image |

☐   13.   Document ID: US 5826057 A

L9: Entry 13 of 43   File: USPT   Oct 20, 1998

US-PAT-NO: 5826057
DOCUMENT-IDENTIFIER: US 5826057 A

TITLE: Method for managing virtual address space at improved space utilization efficiency

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |
| Draw Desc | Image |

☑   14.   Document ID: US 5748976 A

L9: Entry 14 of 43   File: USPT   May 5, 1998

US-PAT-NO: 5748976
DOCUMENT-IDENTIFIER: US 5748976 A

TITLE: Mechanism for maintaining data coherency in a branch history instruction cache

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |
| Draw Desc | Image |

☐   15.   Document ID: US 5701449 A

L9: Entry 15 of 43   File: USPT   Dec 23, 1997

US-PAT-NO: 5701449
DOCUMENT-IDENTIFIER: US 5701449 A

TITLE: Data processor

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |
| Draw Desc | Image |

☐   16.   Document ID: US 5694568 A

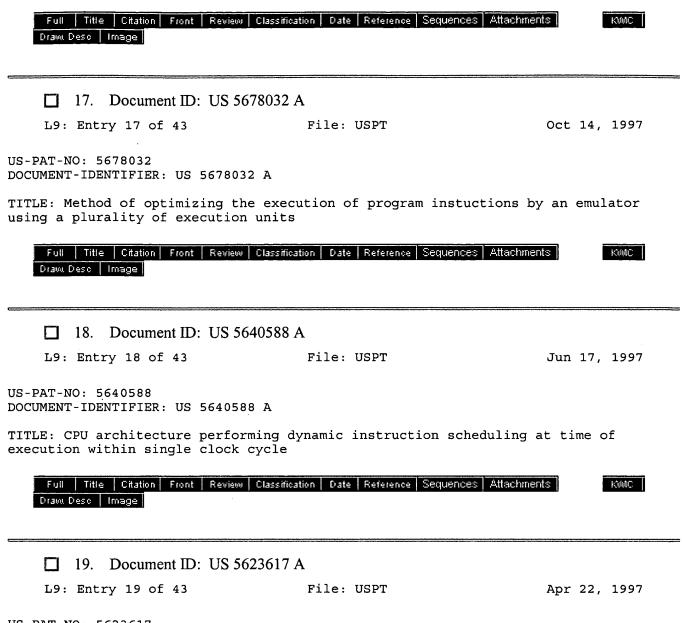L9: Entry 16 of 43   File: USPT   Dec 2, 1997

US-PAT-NO: 5694568
DOCUMENT-IDENTIFIER: US 5694568 A

TITLE: Prefetch system applicable to complex memory access schemes

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |` `KWIC`
`| Draw Desc | Image |`

☐ 17. Document ID: US 5678032 A

L9: Entry 17 of 43   File: USPT   Oct 14, 1997

US-PAT-NO: 5678032
DOCUMENT-IDENTIFIER: US 5678032 A

TITLE: Method of optimizing the execution of program instuctions by an emulator using a plurality of execution units

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |` `KWIC`
`| Draw Desc | Image |`

☐ 18. Document ID: US 5640588 A

L9: Entry 18 of 43   File: USPT   Jun 17, 1997

US-PAT-NO: 5640588
DOCUMENT-IDENTIFIER: US 5640588 A

TITLE: CPU architecture performing dynamic instruction scheduling at time of execution within single clock cycle

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |` `KWIC`
`| Draw Desc | Image |`

☐ 19. Document ID: US 5623617 A

L9: Entry 19 of 43   File: USPT   Apr 22, 1997

US-PAT-NO: 5623617
DOCUMENT-IDENTIFIER: US 5623617 A

TITLE: Method for decoding sequences of guest instructions for a host computer

`| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments |` `KWIC`
`| Draw Desc | Image |`

☐ 20. Document ID: US 5574873 A

L9: Entry 20 of 43   File: USPT   Nov 12, 1996

US-PAT-NO: 5574873
DOCUMENT-IDENTIFIER: US 5574873 A

TITLE: Decoding guest instruction to directly access emulation routines that emulate the guest instructions

| Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | | KWIC |
| Draw Desc | Image |

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Term	Documents
COMPUT$3	0
COMPUT.USPT.	2067
COMPUTA.USPT.	19
COMPUTADO.USPT.	1
COMPUTAK.USPT.	3
COMPUTALK.USPT.	1
COMPUTALL.USPT.	1
COMPUTANK.USPT.	1
COMPUTAP.USPT.	2
COMPUTAR.USPT.	30
COMPUTAS.USPT.	2
((COMPUT$3 OR CALCULAT$3) NEAR4 EFFECTIVE NEAR3 ADDRESS$3 NEAR8 INSTRUCTION$ NEAR5 (FIRST OR SECOND)).USPT.	43

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